UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,848	08/16/2001	Ori Galzur	TSL-097	4561

22888 7590 06/16/2004

BEVER HOFFMAN & HARMS, LLP
TRI-VALLEY OFFICE
1432 CONCANNON BLVD., BLDG. G
LIVERMORE, CA 94550

EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2133	3

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/931,848	Applicant(s) GALZUR ET AL.	
	Examiner John J. Tabone, Jr.	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,15 and 19* is/are rejected.

7)☒ Claim(s) *5, 6, 8-14, 16-18 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 where examined.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference character(s) mentioned in the description: Label is missing for memory device 300 in Fig. 3. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The specification is objected to because of the following informalities:

   i. Page 4, ¶ 7, convention should be conventional.

   ii. Page 5, ¶ 10 last line, "proceeds until and end; and should be an.

iii. Page 10, ¶ 27 last line, "according to know techniques"; know should be known.

iv. Page 11, ¶ 28, control circuit 350 should be 330.

v. Page 11, ¶ 29 first sentence, "with know wafer"; know should be known.

Appropriate correction is required.

Claim Objections

4. Claim 18 is objected to because of the following informalities: This claim is improperly depending on claim 7. For purpose for examination the Examiner is interpreting claim 18 to be dependent on claim 17. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 1, line 6, recites the limitation "first memory". There is insufficient antecedent basis for this limitation in the claim. This limitation should be change to first array.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 7, 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al. (US-5640354), hereafter Jang, in view of Ledford et al. (US-6347056), hereafter Ledford.

Claim 1:

Jang teaches a DRAM having a self-test function includes a row address buffer 52, a row decoder 54, a column address buffer 58, a column decoder 60, and a memory cell array 62. Jang suggests an entry/exit control unit 40 (control circuit) for entering the BIST mode or for existing from the BIST mode in accordance with a combination of externally applied row and column address strobe signals RASB and CASB, a write enable signal WEB, and specific address signals A0, A1, and A2 (receiving self-test instructions). Jang further teaches a data comparison unit 66 (comparator) for comparing the test data (data values) stored in the memory cell array 62, with test data read from the data generating unit 64 (predefined values). (Col. 4, lines 12-21, lines 55-58). Jang does not explicitly teach that the self-test instructions are stored in a first array. However, Jang does suggest that test parameters are externally applied to the entry/exit control unit 40 (control circuit). Ledford suggests algorithmic parameters are stored in non-user addressable locations (first array) Electrically Erasable Array 46 (non-volatile memory cells). Ledford also suggests that the data patterns from the self-test are also written into the Electrically Erasable Array 46 (second array of the non-volatile memory cells). (Col. 5, lines 20-25, 41-46). It would have been obvious to one of

ordinary skill in the art at the time the invention was made Jang's DRAM memory cell array 62 with Ledford's Electrically Erasable Array 46 for storing the test parameters (self-test instructions) and data patterns. The artisan would have been motivated to do so because this would because it would enable Jang to store self-test instructions in memory that would be retained if power was lost. Also, it would lend Jang the flexibility to modify the self-test instructions in the Electrically Erasable Array 46.

Claim 7:

The motivation to modify Jang's DRAM memory cell array 62 with Ledford's Electrically Erasable Array 46 for storing the test parameters (self-test instructions) and data patterns is per claim 1 rejection above. Jang does not explicitly teach that the test parameters are transmitted from a tester. However, Jang does suggests an entry/exit control unit 40 (control circuit) for entering the BIST mode or for existing from the BIST mode in accordance with a combination of externally applied row and column address strobe signals RASB and CASB, a write enable signal WEB, and specific address signals A0, A1, and A2 (receiving self-test instructions). Ledford suggests an external tester (not shown) controls externally applied parameters. (Col. 8, lines 29-33). It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt Jang's entry/exit control unit 40 (control circuit) to include Ledford's tester. The artisan would have been motivated to do so because adding Ledford's tester to Jang's invention would enable Jang to externally modify the self-test instruction written into Ledford's Electrically Erasable Array 46 (see claim 1 rejection).

Claim 15:

The motivation to modify Jang's DRAM memory cell array 62 with Ledford's Electrically Erasable Array 46 for storing the test parameters (self-test instructions) and data patterns is per claim 1 rejection above. Jang teaches a data comparison unit 66 (comparator) for comparing the test data stored in the memory cell array 62, with test data read from the data generating unit 64(reading data values, comparing data values with predefined values). (Col. 4, lines 55-58). Jang does not explicitly teach that the test parameters are transmitted from a tester. However, Jang does suggests an entry/exit control unit 40 (control circuit) for entering the BIST mode or for existing from the BIST mode in accordance with a combination of externally applied row and column address strobe signals RASB and CASB, a write enable signal WEB, and specific address signals A0, A1, and A2 (receiving self-test instructions). Ledford suggests an external tester (not shown) controls externally applied parameters. (Col. 8, lines 29-33). It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt Jang's entry/exit control unit 40 (control circuit) to include Ledford's tester. The artisan would have been motivated to do so because adding Ledford's tester to Jang's invention would enable Jang to externally modify the self-test instruction written into Ledford's Electrically Erasable Array 46 (see claim 1 rejection).

Claim 19:

The motivation to modify Jang's DRAM memory cell array 62 with Ledford's Electrically Erasable Array 46 for writing test parameters (series of self-test instructions) and data patterns is per claim 1 rejection above. Jang suggests under certain input conditions of the address signals A0-A2 the entry/exit control unit 40 outputs a self-test

entry signal S1 (start command). Jang further discloses that BIST mode begins when the self-test entry signal S1 (start command) transitions to a high value. (Col. 5, lines 12-21). Jang further suggests that when all the bits of the counter 46 become a high level the counter 46 generates a test end signal S9 (result data indicating completion). (Col. 6, lines 32,33). Jang teaches that data patterns are written (writing at least one pattern) and read (reading data from second memory cells) in a specific cell of the memory array 62 (now Ledford's Electrically Erasable Array 46) in accordance with a combination of externally applied row and column address strobe signals RASB and CASB, a write enable signal WEB, and specific address signals A0, A1, and A2 (executing self-test instructions). (Col. 4, lines 12-36). Jang further teaches a data comparison unit 66 for comparing the test data read from the memory array 62 (read data) with that of the data generating unit 64 (at least one pattern). (Col. 5, lines 55-60).

Claim 2:

Jang teaches a column address buffer 58 (address buffer) for outputting a column address signal and a row address buffer 52 (address buffer) for outputting a row address signal. Jang also teaches a row decoder 54 connected to the row address buffer 52 (address buffer). Jang further teaches a row control unit 50 (test mode register) for outputting an interior row control signal (row address code) to the row address buffer 52. (Col. 4, lines 12-35).

Claim 3:

Jang teaches a column control unit 56 (counter) for controlling the column address buffer 58 and the column decoder 60 (column decoder). (Col. 4, lines 46, 47).

Claim 4:

Jang teaches a column address buffer 58 (address buffer) for outputting a column address signal and a row address buffer 52 (address buffer) for outputting a row address signal. Jang also teaches a row decoder 54 connected to the row address buffer 52 (address buffer). Jang further teaches a row control unit 50 (counter) for outputting an interior row control signal (row address code) to the row address buffer 52. (Col. 4, lines 12-35). Jang teaches a column control unit 56 (counter) for controlling the column address buffer 58 and the column decoder 60 (column decoder). (Col. 4, lines 46, 47).

Allowable Subject Matter

Claims 5, 6, 8-14, 16-18 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In addition, claim 18 must first satisfy the claim objection set forth in ¶ 4 of this Action.

The following is an Examiner's Statement of Reasons for Allowance:

The prior arts of record teach a non-volatile memory array where algorithmic parameters are stored in non-user addressable locations (first array) Electrically Erasable Array 46 and data values are stored in another area of the array (second array) as well as an entry/exit control unit 40 (control circuit) for receiving externally applied test parameter (self-test instructions) from an external tester. The prior arts of record also teach comparing the data values with predetermined data values. (Per claim

1, 7, 15, and 19). In addition, the prior arts of record teach a row address buffer 52, a row decoder 54, a column address buffer 58, a column decoder 60, a test mode register and a counter, per claims 2-4; Jang et al. (US-5640354) is one example of such prior arts. The prior arts of record, however, fail to teach, singly or in combination, an output controller for registering the self-test instructions and a data bus connected between the output controller and the control circuit per claim 5, a data input buffer connected to the data bus and controlled by the control circuit per claim 6. The prior arts of record also fail to teach, singly or in combination, the method of reading the first instruction by transmitting the first address code to the addressing circuit and reading the first instruction from the first array per claim 8 and reading and verifying the series of self-test instructions from the first memory cells before transmitting a start command per claim 20.

Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100